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In the claims

Please cancel claims 1 - 56, 65, 67, 69 - 76, and 79 - 80 and add the following new claims:

--81. The memory of claim 57 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

82. The memory of claim 81 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

83. The memory of claim 82 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

84. The memory of claim 83 wherein said multiplexers are positioned at every second individual array.

85. The memory of claim 57 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

86. The memory of claim 85 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

87. The memory of claim 85 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

88. The memory of claim 87 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

89. The memory of claim 57 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

90. The memory of claim 89 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

91. The memory of claim 57 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

92. The memory of claim 91 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

93. The memory of claim 91 wherein said plurality of power amplifiers are divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

94. The memory of claim 57 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for

operation in one of separate or concurrent operation to achieve predetermined levels of output power.

95. The memory of claim 94 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

96. The memory of claim 57 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

97. The memory of claim 57 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

98. The memory of claim 57 wherein said memory provides at least 256 meg of storage.

99. The memory of claim 98 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

100. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of pads located centrally with respect to said array blocks;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies located proximate said plurality of pads for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said plurality of peripheral devices.

Cont a2

101. The system claim 100 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

102. The system of claim 101 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

103. The system of claim 102 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

104. The system of claim 103 wherein said multiplexers are positioned at every second individual array.

105. The system of claim 100 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

106. The system of claim 105 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

107. The system of claim 105 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

108. The system of claim 107 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

109. The system of claim 100 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

110. The system of claim 109 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

111. The system of claim 100 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

112. The system of claim 111 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

113. The system of claim 111 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

114. The system of claim 100 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for

operation in one of separate or concurrent operation to achieve predetermined levels of output power.

115. The system of claim 114 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

116. The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

117. The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

118. The system of claim 100 wherein said memory provides at least 256 meg of storage.

119. The system of claim 118 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

120. The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

121. The power distribution bus of claim 120 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the array blocks.

122. The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

123. The power distribution bus of claim 122 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the array blocks.

124. The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

125. The power distribution bus of claim 124 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the array blocks.

126. The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage.

127. The power distribution bus of claim 126 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the array blocks.

128. The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

129. The power distribution bus of claim 128 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the array blocks.

130. The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

131. The power distribution bus of claim 130 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the array blocks.

132. The power distribution bus of claim 58 wherein certain of said first plurality of conductors are for carrying a peripheral voltage.

133. The power distribution bus of claim 132 additionally comprising a plurality of switches each controlling the distribution of the peripheral voltage to one of the array blocks.

134. The power distribution bus of claim 58 wherein said first plurality of conductors extend from an area located centrally with respect to the memory blocks.

135. The power distribution bus of claim 58 additionally comprising a third plurality of conductors running parallel to a plurality of input/output pads for receiving external power from the pads and for supplying the external power to a plurality of voltage supplies located proximate to the pads.

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136. A system for generating and distributing power to a memory device constructed of memory blocks and organized into an array, said system comprising:

a plurality of voltage supplies located centrally with respect to the memory blocks of the array and for producing a plurality of operating voltages; and

a first plurality of conductors forming a web surrounding each of the blocks of the array, one of said conductors being responsive to ground potential, said other conductors being responsive to the plurality of operating voltages.

137. The system of claim 136 wherein one of said plurality of voltage supplies includes a voltage regulator for producing an array voltage and a peripheral voltage.

138. The system of claim 136 wherein one of said plurality of voltage supplies includes a voltage pump for producing a back bias voltage.

139. The system of claim 136 wherein one of said plurality of voltage supplies includes a generator for producing a cellplate and digitline bias voltage.

140. The system of claim 136 wherein one of said plurality of power supplies includes a voltage pump for producing a boosted array voltage.

141. The system of claim 136 additionally comprising a second plurality of conductors extending from said web into each of the memory blocks to form a grid within each of the memory blocks.

142. The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

143. The system of claim 142 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the memory blocks.

144. The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

145. The system of claim 144 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the memory blocks.

146. The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

147. The system of claim 146 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the memory blocks.

148. The system claim 141 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage.

149. The system of claim 148 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the memory blocks.

150. The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

151. The system of claim 150 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the memory blocks.

152. The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

153. The system of claim 152 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the memory blocks.

154. The system of claim 141 additionally comprising a plurality of input/output pads for receiving external power and positioned proximate to said plurality of voltage supplies.

155. The system of claim 154 additionally comprising a third plurality of conductors for connecting certain of said plurality of input/output pads to said plurality of voltage supplies.

156. The system of claim 155 wherein certain of said third plurality of conductors are for carrying an external voltage.

157. The system of claim 155 wherein certain of said third plurality of conductors are for carrying a pad driver external voltage.

158. The system of claim 155 wherein certain of said third plurality of conductors are for carrying a pad driver ground potential.

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159. A method of generating and distributing voltages to a dynamic random access memory device having a plurality of memory blocks arranged in an array and a plurality of pads located centrally of said array of memory blocks, said method comprising the steps of:

generating a plurality of voltages with a plurality of voltage supplies positioned proximate to the plurality of pads;

distributing said plurality of voltages through a web surrounding each of the blocks of the array, and

distributing certain of said plurality of voltages into each of the memory blocks through a second plurality of conductors extending from said web into each of the memory blocks.

160. The method of claim 159 additionally comprising the step of distributing to the voltage supplies through a third plurality of conductors certain voltages available at the pads.

161. The method of claim 159 additionally comprising the step of controlling the distribution of said plurality of voltages with a plurality of switches.

162. The memory of claim 59 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

163. The memory of claim 162 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

164. The memory of claim 59 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of output power.

165. The memory of claim 164 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said

secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

166. The memory of claim 59 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

167. The memory of claim 59 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

168. The memory of claim 59 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

169. The memory of claim 168 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

170. The memory of claim 169 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

171. The memory of claim 170 wherein said multiplexers are positioned at every second individual array.

172. The memory of claim 59 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Cont a2

173. The memory of claim 172 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

174. The memory of claim 172 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

175. The memory of claim 174 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

176. The memory of claim 59 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

177. The memory of claim 176 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

178. The memory of claim 59 wherein said memory provides at least 256 meg of storage.

179. The memory of claim 178 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 Meg of storage.

180. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and wherein said power amplifiers are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

181. The system of claim 180 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

182. The system of claim 181 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

183. The system of claim 180 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of output power.

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184. The system of claim 183 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

185. The system of claim 180 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

186. The system of claim 180 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

187. The system of claim 180 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

188. The system of claim 187 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

189. The system of claim 188 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

190. The system of claim 189 wherein said multiplexers are positioned at every second individual array.

191. The system of claim 180 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

cont a2

192. The system of claim 191 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

193. The system of claim 191 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

194. The system of claim 193 wherein said individual arrays of memory cells include memory cells arranged in rows and column, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

195. The system of claim 180 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

196. The system of claim 195 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to certain of said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

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197. The system of claim 180 wherein said memory provides at least 256 meg of storage.

198. The system of claim 197 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

199. The voltage regulator of claim 60 wherein said plurality of power amplifiers is divided into a plurality of groups for one of independent and concurrent operation among said groups.

200. The voltage regulator of claim 60 wherein each of said plurality of power amplifiers comprises an amplifier portion and a boost circuit that is operable to increase the slew rate of said amplifier portion in response to said control signals.

201. The voltage regulator of claim 60 additionally comprising a booster amplifier for supplying additional power to the dynamic random access memory in response to said control signals reflecting a predetermined operating condition.

202. The voltage regulator of claim 201 wherein said booster amplifier has an output connected through an impedance with an output of said power amplifiers.

203. The voltage regulator of claim 201 additionally comprising a standby amplifier for supplying power in response to said control signals reflecting periods in which said plurality of power amplifiers and said booster amplifier are not operating.

204. The voltage regulator of claim 201 wherein said booster amplifier is designed to operate on a bias current less than a bias current required for each of said plurality of power amplifiers.

205. The voltage regulator of claim 204 wherein said standby amplifier is designed to operate on a bias current less than said bias currents required for each of said plurality of power amplifiers and said booster amplifier.

206. An amplifier portion of a voltage regulator for a dynamic random access memory, said amplifier portion comprising:

a plurality of power amplifiers divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of power output to the dynamic random access memory.

Cont A2

207. The amplifier portion of claim 206 additionally comprising a booster amplifier for supplying additional power in response to a predetermined operating condition.

208. The amplifier portion of claim 207 additionally comprising a standby amplifier for maintaining a nominal level of power output to the dynamic random access memory when said plurality of power amplifiers and said booster amplifier are not operating.

209. The amplifier portion of claim 206 wherein each of said plurality of power amplifiers has a gain greater than one.

210. The amplifier portion of claim 206 wherein each of said plurality of power amplifiers comprises an amplifier portion and a boost circuit that is operable to increase the slew rate of said amplifier portion in response to a predetermined operating condition..

211. A voltage regulator for a dynamic random access memory, comprising:

a circuit for generating a reference voltage from an externally supplied voltage;

an amplifier for amplifying said reference voltage with a gain greater than unity to generate an internal supply voltage available on first and second buses; and

control logic for generating control signals for controlling said amplifier.

212. The voltage regulator of claim 211 wherein said amplifier comprises a plurality of individual amplifiers arranged substantially in parallel between said circuit for generating a reference voltage and said first bus.

213. The voltage regulator of claim 212 wherein said first bus carries an array voltage.

214. The voltage regulator of claim 213 wherein said first bus is connected to said second bus through an impedance.

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215. The voltage regulator of claim 214 wherein said second bus carries a peripheral voltage.

216. The voltage regulator of claim 211 wherein said amplifier comprises at least one power amplifier, at least one booster amplifier, and at least one standby amplifier, wherein said voltage regulator has reduced operating current requirements by allowing selective operation of the individual amplifiers in one of individual and predetermined combinations.

217. A method of operating a voltage regulator for a dynamic random access memory, comprising the steps of:

generating a reference voltage from an externally supplied voltage;

amplifying said reference voltage with a gain greater than unity to generate an internal supply voltage available on a bus; and

generating control signals for controlling said step of amplifying

218. A method of operating an amplifier portion of a voltage regulator for a dynamic random access memory, said method comprising the steps of:

operating at least one power amplifier during periods of memory array operations;

operating, independently of the operating of the at least one power amplifier, at least one booster amplifier during periods of voltage pump operations; and

operating a standby amplifier at a low maintenance current level regardless of the state of operation of the power amplifier and booster amplifier.

219. The method of claim 218 wherein said step of operating the standby amplifier includes operating the standby amplifier at a current level that is less than that required for operating the at least one power amplifier.

220. The method of claim 218 wherein said step of operating the at least one power amplifier comprises the step of operating a plurality of power amplifiers in groups to match the power produced to the power required by the memory.

221. The method of claim 220 wherein said step of operating a plurality of power amplifiers in groups includes operating a plurality of power amplifiers in groups to perform refresh operations at various rates.

222. The method of claim 218 wherein said steps of operating at least one power amplifier and operating at least one booster amplifier are carried out while maintaining an impedance between the respective outputs of the at least one power amplifier and the at least one booster amplifier to avoid transfer of transients.

223. A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage; and

a unity gain amplifier responsive to said reference signal for producing the reference voltage.

224. The voltage reference circuit of claim 223 wherein said active reference circuit comprises a current source providing current to a diode stack having an adjustable impedance for producing said reference signal.

225. The voltage reference circuit of claim 224 wherein said diode stack includes a plurality of transistors connected in series, with each transistor's gate connected to a common potential, and a plurality of switches each for selectively shunting one of said transistors.

226. The voltage reference circuit of claim 225 wherein said switches are controlled by fuses, and wherein opening certain of said fuses turns its associated switch on, and wherein opening certain other of said fuses turns its associated switch off.

227. The voltage reference circuit of claim 226 wherein said plurality of transistors includes a first plurality of field effect transistors and wherein said plurality of switches includes a second plurality of field effect transistors.

228. The voltage reference circuit of claim 223 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value.

229. The voltage reference circuit of claim 228 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

230. The voltage reference circuit of claim 229 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

cont A2

231. A voltage reference circuit in combination with a power amplifier, said combination comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship to the external voltage;

a unity gain amplifier responsive to said reference signal for producing a reference voltage; and

a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide an output voltage.

232. The combination of claim 231 additionally comprising a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value.

233. The combination of claim 232 wherein said circuit for supplying includes a switch for shorting a bus carrying the external voltage with a bus carrying the output voltage.

234. The combination of claim 232 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a second predetermined value.

235. The combination of claim 234 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

236. The combination of claim 235 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

237. The combination of claim 234 wherein said combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range, increases at a second slope substantially less than a slope of the external voltage during an operating range, and increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage.

238. A voltage regulator for a dynamic random access memory for supplying an output voltage in response to an external voltage, and wherein the output voltage has a first characteristic when the external voltage is in a powerup range, has a second characteristic when the external voltage is in an operating range, and has a third characteristic when the external voltage is in a burn-in range, said regulator comprising:

a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value defining the powerup range;

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage;

a unity gain amplifier responsive to said reference signal for producing a reference voltage when the external voltage is above said first predetermined value;

a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide the output voltage when said circuit for supplying is not supplying the external voltage as the output voltage; and

a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds said second predetermined value defining the burn-in range.

239. The voltage regulator of claim 238 wherein said active reference circuit comprises a current source for presenting a current at a circuit node and a circuit for providing an

impedance between said node and a reference potential, said reference signal being available at said node.

240. The voltage regulator of claim 239 wherein said circuit for providing an impedance includes a circuit for adjusting the impedance to modify said reference signal available at said node.

241. The voltage regulator of claim 240 wherein said circuit for providing an impedance includes a plurality of transistors connected in series, with each transistor's gate connected to a common potential, and a plurality of switches each for selectively shunting one of said transistors.

242. The voltage regulator of claim 241 wherein said switches are controlled by fuses, and wherein opening certain of said fuses turns its associated switch on, and wherein opening certain other of said fuses turns its associated switch off.

243. The voltage regulator of claim 242 wherein said plurality of transistors includes a first plurality of field effect transistors and wherein said plurality of switches includes a second plurality of field effect transistors.

244. The voltage regulator of claim 238 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

245. The voltage regulator of claim 244 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

246. The voltage regulator of claim 238 wherein said circuit for supplying includes a switch for shorting a bus carrying the external voltage with a bus carrying the output voltage.

247. A method of supplying an output voltage in response to an external voltage, and wherein the output voltage has a first characteristic when the external voltage is in a powerup range, has a second characteristic when the external voltage is in an operating range, and has a third characteristic when the external voltage is in a burn-in range, said method comprising the steps of:

supplying the external voltage as the output voltage when the external voltage is below a first predetermined value defining the powerup range;

producing a reference signal having a desired relationship with the external voltage;

amplifying the reference signal with a unity gain amplifier for producing a reference voltage when the external voltage is above said first predetermined value;

amplifying the reference voltage by a factor greater than unity to provide the output voltage when the external voltage is not being supplied as the output voltage; and

pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds said second predetermined value defining the burn-in range.

248. The method of claim 247 wherein said step of producing a reference signal includes the steps of generating a current related to the external voltage, applying the current to a circuit node, and draining the current from the circuit node through an adjustable impedance.

249. The method of claim 248 additionally comprising the step of adjusting the impedance to modify the reference signal.

250. The method of claim 249 wherein said step of adjusting the impedance includes the step of opening a fuse.

251. The memory of claim 61 wherein said logic disables the power amplifier associated with an array block that has had its power distribution switch opened.

252. The memory of claim 61 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said individual arrays are organized to form said array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

253. The memory of claim 252 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array

blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

254. The memory of claim 253 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

cont a2

255. The memory of claim 254 wherein said multiplexers are positioned at every second individual array.

256. The memory of claim 61 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

257. The memory of claim 256 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

258. The memory of claim 256 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

259. The memory of claim 258 wherein said array of memory cells includes memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

260. The memory of claim 61 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

261. The memory of claim 260 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

cont a2

262. The memory of claim 61 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

263. The memory of claim 61 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

264. The memory of claim 263 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

265. The memory of claim 61 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

266. The memory of claim 61 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

267. The memory of claim 61 wherein said memory provides at least 256 meg of storage.

268. The memory of claim 267 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

269. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells configured in separately controllable array blocks;

a plurality of peripheral devices responsive to external signals for writing data into said array blocks and for reading data out of said array blocks;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and at least one of said power amplifiers being associated with each of said array blocks;

a plurality of power distribution switches; and

a power distribution bus for delivering said plurality of supply voltages to said array blocks through said plurality of switches and to said plurality of peripheral devices, and wherein said plurality of peripheral devices includes logic for controlling each of said plurality of switches and for controlling the state of each of said power amplifiers.

270. The system of claim 269 wherein said logic disables the power amplifier associated with an array block that has had its power distribution switch opened.

271. The system of claim 269 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said individual arrays are organized to form said array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array

blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

272. The system of claim 271 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

273. The system of claim 272 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

274. The system of claim 273 wherein said multiplexers are positioned at every second individual array.

275. The system of claim 269 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

276. The system of claim 275 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

277. The system of claim 275 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

278. The system of claim 277 wherein said array of memory cells includes memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

279. The system of claim 269 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

280. The system of claim 279 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

281. The system of claim 269 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

282. The system of claim 269 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

283. The system of claim 282 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

284. The system of claim 269 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

285. The system of claim 269 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

286. The system of claim 269 wherein said memory provides at least 256 meg of storage.

287. The system of claim 286 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

288. The voltage regulator of claim 62 wherein each array block has a capacitance associated therewith, and wherein said control circuitry disables power amplifiers in response to array blocks being disabled so as to maintain a predetermined ratio of the total remaining capacitance to the number of operational power amplifiers.

289. The voltage regulator of claim 288 wherein said predetermined ratio is approximately 0.25 nanofarads per operational power amplifier.

290. The voltage regulator of claim 62 wherein said multiple power amplifiers include twelve amplifiers, and wherein eight of said power amplifiers are each associated with one of eight array blocks.

291. Voltage regulator circuitry for inclusion in a dynamic random access memory, said circuitry comprising:

independent circuits for developing a supply voltage for a plurality of memory array blocks of the dynamic random access memory; and

a control circuit for receiving a signal when one of the memory array blocks is disabled and for producing control signals in response thereto for disabling one of said independent circuits.

292. The circuitry of claim 291 wherein each array block has a capacitance associated therewith, and wherein said control circuit produces control signals for disabling certain

independent circuits in response to array blocks being disabled so as to maintain a predetermined ratio of the total remaining capacitance to the total number of operational independent circuits.

293. The circuitry of claim 292 wherein said predetermined ratio is approximately 0.25 nanofarads per operational module.

294. A method of operating an amplifier portion of a voltage regulator for a dynamic random access memory divided into array blocks, said amplifier portion having a number of individual power amplifiers, said method comprising the steps of:

operating at least one power amplifier for each array block during periods when operations are performed by the memory;

determining when an array block has become disabled; and

disabling at least one power amplifier for each disabled array block.

295. The method of claim 294 wherein each array block has a capacitance associated therewith, and wherein said step of disabling at least one power amplifier includes the step of maintaining a predetermined ratio of the total remaining capacitance to non-disabled power amplifiers.

296. The method of claim 295 wherein said predetermined ratio is approximately 0.25 nanofarads per non-disabled power amplifier.

297. A method of operating an amplifier portion of a voltage regulator for a dynamic random access memory divided into eight array blocks, said amplifier portion having a number of individual power amplifiers, said method comprising the steps of:

operating at least one power amplifier for each of the eight array blocks during periods when operations are performed on the memory;

operating the remaining power amplifiers in one of individual and group modes depending on the power requirements of the memory;

determining when an array block has become disabled; and

disabling the power amplifier associated with the disabled array block.

298. The power supply of claim 63 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of the plurality of array blocks.

299. The power supply of claim 298 including circuits for disabling said at least one power amplifier associated with each of the plurality of array blocks when the array block associated therewith is disabled.

300. The power supply of claim 299 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

301. The power supply of claim 63 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output.

302. The power supply of claim 301 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

303. The power supply of claim 302 wherein the first type of refresh mode includes a 4k refresh mode and wherein said second type of refresh mode includes an 8k refresh mode.

304. The power supply of claim 63 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

305. The power supply of claim 63 wherein said plurality of voltage supplies includes a voltage regulator, a first and a second voltage pumps, and a generator for producing a bias voltage, said memory additionally comprising a powerup sequence circuit for controlling

powering up of said voltage regulator, said voltage pumps, and said generator for producing a bias voltage in response to an external voltage.

306. The memory of claim 64 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

307. The memory of claim 306 wherein the first type of refresh mode includes a 4k refresh mode and wherein the second type of refresh mode includes an 8k refresh mode.

308. The memory of claim 64 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator including a plurality of power amplifiers, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

309. The memory of claim 308 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

310. The memory of claim 309 wherein said plurality of power amplifiers is divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

311. The memory of claim 64 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

312. The memory of claim 311 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

313. The memory of claim 64 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual

arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

314. The memory of claim 313 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

315. The memory of claim 314 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

316. The memory of claim 314 wherein said multiplexers are positioned at every other individual array.

317. The memory of claim 64 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

318. The memory of claim 317 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

319. The memory of claim 317 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

320. The memory of claim 319 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

321. The memory of claim 64 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

322. The memory of claim 321 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

323. The memory of claim 64 wherein said memory provides at least 256 meg of storage.

324. The memory of claim 323 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

325. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage pump comprised of a plurality of voltage pump circuits and

wherein said voltage pump circuits are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

326. The system of claim 325 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Cont a2

327. The system of claim 326 wherein the first type of refresh mode includes a 4k refresh mode and wherein the second type of refresh mode includes an 8k refresh mode.

328. The system of claim 325 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator including a plurality of power amplifiers, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

329. The system of claim 328 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

330. The system of claim 329 wherein said plurality of power amplifiers is divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

331. The system of claim 325 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

332. The system of claim 325 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

333. The system of claim 325 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual

arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

334. The system of claim 333 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

cont a2

335. The system of claim 334 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

336. The system of claim 334 wherein said multiplexers are positioned at every other individual array.

337. The system of claim 325 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

338. The system of claim 337 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

339. The system of claim 337 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

340. The system of claim 339 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

341. The system of claim 325 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Cont A2

342. The system of claim 341 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

343. The system of claim 325 wherein said memory provides at least 256 meg of storage.

344. The system of claim 343 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

345. An output portion of a voltage pump for a dynamic random access memory, comprising:

a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of power output to the dynamic random access memory.

346. The output portion of claim 345 wherein each of said plurality of voltage pump circuits includes two substantially identical pump portions operating in tandem in response to an externally supplied clock signal.

347. The output portion of claim 345 wherein said plurality of voltage pump circuits includes twelve pump circuits all of which are operable when the dynamic random access memory is in a first type of refresh mode and wherein only a portion of said twelve pump circuits are operable when the dynamic random access memory is in a second type of fresh mode.

348. The output portion of claim 347 wherein six of said pump circuits are in a primary group and six of said pump circuits are in a secondary group, and wherein both groups of pump circuits are operable in response to the first type of refresh mode and wherein only said primary group of pump circuits is operable in response to the second type of refresh mode.

349. The output portion of claim 348 wherein both groups of pump circuits are operable in response to a 4k refresh mode and wherein only said primary group of pump circuits is operable in response to an 8k refresh mode.

350. The memory of claim 66 wherein said voltage generator is of the type which utilizes a pullup and a pulldown current for regulation purposes, said memory additionally comprising:

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

351. The memory of claim 66 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is

organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

352. The memory of claim 351 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Cont A2

353. The memory of claim 352 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

354. The memory of claim 353 wherein said multiplexers are positioned at every second individual array.

355. The memory of claim 66 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

356. The memory of claim 355 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

357. The memory of claim 355 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

358. The memory of claim 357 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

359. The memory of claim 66 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Cont A2

360. The memory of claim 359 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

361. The memory of claim 66 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

362. The memory of claim 361 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

363. The memory of claim 361 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

364. The memory of claim 66 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for

operation in one of separate and concurrent operation to achieve predetermined levels of output power.

365. The memory of claim 364 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

366. The memory of claim 66 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

367. The memory of claim 366 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

368. The memory of claim 66 wherein said memory provides at least 256 meg of storage.

369. The memory of claim 368 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

370. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices responsive to external signals for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices, one of said plurality of voltage supplies including a voltage generator producing an output voltage;

a voltage detection circuit responsive to said output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication of the stability of the voltage generator.

371. The system of claim 370 wherein said voltage generator is of the type which utilizes a pullup and a pulldown current for regulation purposes, said memory additionally comprising:

cont a2

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

372. The system of claim 370 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

373. The system of claim 372 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

374. The system of claim 373 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

375. The system of claim 374 wherein said multiplexers are positioned at every second individual array.

376. The system of claim 370 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

cont a2

377. The system of claim 376 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

378. The system of claim 376 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

379. The system of claim 378 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

380. The system of claim 370 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

381. The system of claim 380 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

382. The system of claim 370 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

383. The system of claim 382 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

384. The system of claim 382 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

385. The system of claim 370 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

386. The system of claim 385 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

387. The system of claim 370 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

388. The system of claim 387 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

389. The system of claim 370 wherein said memory provides at least 256 meg of storage.

390. The system of claim 389 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

391. A stability sensor for a voltage generator generating an output voltage, comprising:

a voltage detection circuit responsive to the output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication of the stability of the voltage generator.

392. The stability sensor of claim 391 wherein said voltage detection circuit includes:

a first transistor responsive to the output voltage for producing said overvoltage signal indicative of whether the output voltage is greater than an upper limit of said first predetermined range; and

a second transistor responsive to the output voltage for producing said undervoltage signal indicative of whether the output voltage is less than a lower limit of said first predetermined range.

393. The stability sensor of claim 391 wherein said voltage generator is of the type which utilizes a pullup and a pulldown current for regulation purposes, said sensor further comprising:

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

394. The stability sensor of claim 393 wherein said pullup current monitor includes:

a source circuit for sourcing current, each source current being indicative of the present pullup current;

a sink circuit for sinking current;

an RC time constant circuit connected between said source circuit and said sink circuit such that each sink current is indicative of a previous pullup current;

a positive differential current circuit responsive to the source current and the sink current for generating said first pullup signal indicative of whether the present pullup current is greater than the previous pullup current; and

a negative differential current circuit responsive to the source current and the sink current for generating said second pullup signal indicative of whether the present pullup current is less than the previous pullup current.

395. The stability sensor of claim 394 wherein said sink circuit includes a transistor controlled by said RC time constant circuit.

396. The stability sensor of claim 394 wherein said RC time constant circuit includes a resistor in combination with a capacitor, and wherein a charge stored by said capacitor is responsive to the difference between the source current and the sink current.

397. The stability sensor of claim 394 wherein said positive differential circuit includes a resistor connected to produce a voltage indicative of the difference between the source current and the sink current and an inverter responsive to said voltage.

398. The stability sensor of claim 394 wherein said negative differential circuit includes a resistor connected to produce a voltage indicative of the difference between the source current and the sink current and a pair of series connected inverters responsive to said voltage.

399. The stability sensor of claim 393 wherein said pulldown current monitor includes:

a sink circuit for sinking current, each sink current being indicative of the present pulldown current;

a source circuit for sourcing current;

an RC time constant circuit connected between said sink circuit and said source circuit such that each source current is indicative of a previous pulldown current;

a positive differential current circuit responsive to the sink current and the source current for generating said first pulldown signal indicative of whether the present pulldown current is greater than the previous pulldown current; and

a negative differential current circuit responsive to the sink current and the source current for generating said second pulldown signal indicative of whether the present pulldown current is less than the previous pulldown current.

400. The stability sensor of claim 398 wherein said source circuit includes a transistor controlled by said RC time constant circuit.

401. The stability sensor of claim 399 wherein said RC time constant circuit includes a resistor in combination with a capacitor, and wherein a charge stored by said capacitor is responsive to the difference between the sink current and the source current.

402. The stability sensor of claim 399 wherein said positive differential circuit includes a resistor connected to produce a voltage indicative of the difference between the sink current and the source current and an inverter responsive to said voltage.

403. The stability sensor of claim 399 wherein said negative differential circuit includes a resistor connected to produce a voltage indicative of the difference between the sink current and the source current and a pair of series connected inverters responsive to said voltage.

404. The memory of claim 68 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

405. The memory of claim 404 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

406. The memory of claim 405 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

407. The memory of claim 406 wherein said multiplexers are positioned at every second individual array.

408. The memory of claim 68 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of

peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

409. The memory of claim 408 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

410. The memory of claim 408 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

411. The memory of claim 410 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

412. The memory of claim 68 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

413. The memory of claim 412 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

414. The memory of claim 68 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

415. The memory of claim 414 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

416. The memory of claim 414 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

417. The memory of claim 68 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

418. The memory of claim 417 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

419. The memory of claim 68 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

420. The memory of claim 68 wherein said powerup sequence circuit controls the powering up of certain of said plurality of voltage supplies in response to an externally supplied voltage.

421. The memory of claim 68 wherein said memory provides at least 256 meg of storage.

422. The memory of claim 421 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

423. A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

a powerup sequence circuit for controlling the powering up of certain of the plurality of voltage supplies in response to the condition of previously powered up voltage supplies.

cont a2

424. The system of claim 423 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

425. The system of claim 424 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

426. The system of claim 425 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

427. The system of claim 426 wherein said multiplexers are positioned at every second individual array.

428. The system of claim 423 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

429. The system of claim 428 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

430. The system of claim 428 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

431. The system of claim 430 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

432. The system of claim 423 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

433. The system of claim 432 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

434. The system of claim 423 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage

regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

435. The system of claim 434 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

436. The system of claim 434 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

437. The system of claim 423 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

438. The system of claim 437 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

439. The system of claim 423 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

440. The system of claim 423 wherein said powerup sequence circuit controls the powering up of certain of said plurality of voltage supplies in response to an externally supplied voltage.

441. The system of claim 423 wherein said memory provides at least 256 meg of storage.

442. The system of claim 441 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

443. A device responsive to first and second external signals for controlling a power up of a first voltage supply, comprising:

a first circuit responsive to the first external signal for producing a first output signal indicative of whether the first external signal satisfies a predetermined condition; and

a second circuit responsive to the first output signal and the second external signal for producing a first enable signal to enable the first voltage supply.

444. The device of claim 443, wherein said first output signal is indicative of the first external signal being greater than a first predetermined voltage.

445. The device of claim 444, wherein said first predetermined voltage is approximately two volts.

446. The device of claim 444, wherein said first circuit includes:

a first voltage detector responsive to the first external signal for producing a first signal indicative of the first external signal being greater than said first predetermined voltage;

a second voltage detector responsive to the first external signal for producing a second signal indicative of the first external signal being greater than said first predetermined voltage; and

a logic circuit responsive to said first and second signals for producing said first output signal.

447. The device of claim 446, wherein said first voltage detector includes:

a voltage limiting circuit responsive to the first external signal for producing a threshold signal indicative of whether the first external signal is above a second predetermined voltage; and

a signal generating circuit responsive to the first external signal, said threshold signal, and said first predetermined voltage for producing said first signal.

448. The device of claim 447, wherein said second predetermined voltage is approximately 0.7 volts.

449. The device of claim 447, wherein said voltage limiting circuit includes:

a resistor having a first end and a second end, said first end in communication with the first external signal;

a plurality of series-connected, p-channel transistors each having a gate terminal in communication with a reference potential, with one of said transistors having a source terminal in communication with said second end of said resistor for producing said threshold signal, and

another of said transistors having a drain terminal in communication with said reference potential, said transistors being capable of being shorted across their source and drain terminals to change the value of said threshold signal.

450. The device of claim 449, wherein said signal generating circuit includes:

a resistor having a first end and a second end, said first end in communication with a reference potential; and

a p-channel transistor having a source terminal in communication with the first external signal, a gate terminal in communication with the threshold signal, and a drain terminal in communication with said second end of said resistor for producing said first signal.

451. The device of claim 447, wherein said second voltage detector includes:

a voltage limiting circuit responsive to the first external signal for producing a threshold signal indicative of whether the first external signal is above a second predetermined voltage;

a signal generating circuit responsive to the first external signal, said threshold signal, and said first predetermined voltage for producing said second signal.

452. The device of claim 451, wherein said second predetermined voltage is approximately 0.7 volts.

453. The device of claim 451, wherein said voltage limiting circuit includes:

a resistor having a first end and a second end, said first end in communication with a reference potential;

a plurality of series-connected, n-channel transistors each having a gate terminal in communication with the first external signal, with one of said transistors having a drain terminal

in communication with the first external signal, and another of said transistors having a source terminal in communication with said second end of said resistor for producing the threshold signal, said transistors being capable of being shorted across their source and drain terminals to change the value of said threshold signal.

454. The device of claim 453, wherein said signal generating circuit includes:

a resistor having a first end and a second end, said first end in communication with the first external signal; and

an n-channel transistor having a source terminal in communication with the reference potential, a gate terminal in communication with said threshold signal, and a drain terminal in communication with said second end of said resistor for producing said second signal.

Cont A2

455. The device of claim 446, wherein said logic circuit includes:

first and second series connected inverters for receiving said first signal;

a third inverter for receiving said second signal;

a NAND gate responsive to said series connected first and second inverters and said third invertor; and

a fourth inverter responsive to said NAND gate for producing said first output signal.

456. The device of claim 443, additionally comprising a reset circuit interposed between said first and second circuits for receiving said first output signal from said first circuit and for terminating said first output signal when predetermined stability requirements are not meet.

457. The device of claim 456, wherein said predetermined stability requirements include said first output signal remaining within a predetermined range for approximately one hundred nanoseconds.

458. The device of claim 456 wherein said reset circuit includes:

a plurality of series-connected buffer gates with a first one of said buffer gates responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffer gates.

459. The device of claim 458, wherein said reset circuit includes:

a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with said last one of said series-connected buffer gates, and an output terminal; and

an inverter having an input terminal in communication with said output terminal of said NAND gate, and an output terminal at which said first output signal is available.

460. The device of claim 458 wherein said reset circuit further includes a reset logic gate responsive to said first output signal for producing a reset signal for resetting said buffer gates to a predetermined state.

461. The device of claim 443, wherein said second circuit includes:

a logic circuit responsive to said first output signal and the second external signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said first enable signal.

462. The device of claim 461, wherein said logic circuit includes a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with the second external signal, and an output terminal for producing said output signal of said logic circuit.

463. The device of claim 443, wherein said device is responsive to a third external signal for controlling the power up sequence of a second voltage supply, said device comprising:

a third circuit responsive to said first output signal, the second external signal, and the third external signal for producing a second enable signal to enable the second voltage supply.

464. The device of claim 463, wherein said third circuit includes: